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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/089,312	06/02/1998	STEWART FINDLATER	CISCP035	2703

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EXAMINER	
HOM, SHICK C	

ART UNIT	PAPER NUMBER
2666	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/089,312	FINDLATER ET AL.	
	Examiner	Art Unit	
	Shick C Hom	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3, 4-6, 9-10, 13-17* is/are rejected.

7)☐ Claim(s) *2,7,8,11,12,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. The request for continued examination (RCE) under 37 CFR 1.114 filed on 10/7/04 is acknowledged.

Response to Arguments

2. Applicant's arguments with respect to claims 1-17 and 19-20 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

3. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the [illegible]

Claim Rejections - 35 USC § 112

4. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 3 line 2 which recite "the receive data line" lacks clear antecedent basis because no receive data line

have been previously recited in the claims and therefore the limitation is not clearly understood.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1, 4-6, 9-10, and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (6,044,087) in view of Biggs et al. (5,535,398).

Regarding claims 1, 15, and 16:

Muller et al. disclose the method of communicating between a media access control layer (MAC) and a physical layer (PHY) (in Fig. 3a see communication between the MAC 320 and PHY 350 and in col. 4 line 57 to col. 5 line 4 which recite the interface between the MAC circuitry and the physical layer device), comprising: a common clock (see col. 1 lines 46-62 which recite the clock), receiving a first time-division multiplexed signal (see col. 5 line 53 to col. 6 line 7 which recite the transmission and reception of multiplexed data); receiving a plurality of time-division multiplexed receive control signals (see col. 5 lines 5-24 which recite multiplexing being performed on the data control and clock signals clearly anticipate receiving multiplexed control signals); sending a second time-division multiplexed signal (see col. 5 line 53 to col. 6 line 7 which recite the transmission and reception of multiplexed data); sending a plurality of time-division multiplexed transmit control signals (see col. 5 lines 5-24 which recite multiplexing being performed on the data

control and clock signals clearly anticipate receiving multiplexed control signals), wherein the receive control signals include a receive data valid signal and a receive error signal time-division multiplexed together (see Figs. 4a-b and col. 6 lines 8-47 which recite the receive data valid and receive error signals being multiplexed) and the transmit control signals include a transmit enable signal and a transmit error signal time-division multiplexed together (see Figs. 3a-b, col. 5 line 53 to col. 6 line 7 and col. 6 lines 33-47 which recite the transmit enable and transmit coding error signals being multiplexed).

For claims 1, 15, and 16 Muller et al. disclose all the subject matter of the claimed invention with the exception of using a single pin for receiving the multiplexed signal, the use of a single pin for receiving the multiplexed control signals, the use of a single pin for sending the multiplexed signal, and the use a single pin for sending the multiplexed control signals.

Biggs et al. from the same or similar fields of endeavor teach that it is known to use a single pin for receiving the multiplexed signals, the use of a single pin for receiving the multiplexed control signals, the use of a single pin for sending the multiplexed signals, and the use

a single pin for sending the multiplexed control signals (see col. 1 lines 38-48 which recite multiplexing functions on a same pin and further, col. 5 lines 22-39 which recite the power and control pin clearly anticipate the use a single pin for receiving or sending multiplexed control signals). Thus, it would have been obvious to the person having ordinary skill in the art at the time the invention was made to use a single pin for receiving the multiplexed signals, to use a single pin for receiving the multiplexed control signals, to use a single pin for sending the multiplexed signal, and to use a single pin for sending the multiplexed control signals as taught by Biggs et al. in the communications method of Muller et al. The use a single pin for receiving the multiplexed signals, the use of a single pin for receiving the multiplexed control signals, the use of a single pin for sending the multiplexed signals, and the use a single pin for sending the multiplexed control signals can be implemented by connecting the received multiplexed signal, the received multiplexed control signals, the sending multiplexed signals, and the sending multiplexed control signals of Muller et al. into a single receive data pin, a single receive control pin, a single transmit data pin, and a

single transmit control pin, respectively, of Biggs et al. The motivation using a single pin for receiving the multiplexed signals, the use of a single pin for receiving the multiplexed control signals, the use of a single pin for sending the multiplexed signals, and the use a single pin for sending the multiplexed control signals as taught by Biggs et al. in the communication method of Muller et al. being that it provides more efficiency for the method of interfacing between the MAC and PHY since the use of a single pin for multiplexed signals reduces the pin count of the circuit.

Regarding claim 4:

Muller et al. disclose wherein the time-division multiplexed receive control signals includes 4 bit segments of the receive data line and wherein each 4 bit segment includes a receive data valid bit (col. 5 line 53 to col. 6 line 32, Figs. 4a-b, and col. 6 lines 8-47).

Regarding claim 5:

Muller et al. disclose wherein the time-division multiplexed receive control signals includes 4 bit segments and wherein each 4 bit segment includes a receive error bit (col. 5 line 53 to col. 6 line 32, Figs. 4a-b, and col. 6 lines 8-47).

Regarding claim 6:

Muller et al. disclose wherein the time-division multiplexed receive control signals includes 4 bit segments and wherein each 4 bit segment includes a carrier sense bit (col. 5 line 53 to col. 6 line 32, Figs. 4a-b, and col. 5 lines 25-43).

Regarding claim 9:

Muller et al. disclose wherein the time-division multiplexed transmit control signals includes 4 bit segments and wherein each 4 bit segment includes a transmit enable bit (col. 5 line 53 to col. 6 line 32, Figs. 3a-b, col. 5 line 53 to col. 6 line 7, and col. 6 lines 33-47).

Regarding claim 10:

Muller et al. disclose wherein the time-division multiplexed transmit control signals includes 4 bit segments and wherein each 4 bit segment includes a transmit error bit (col. 5 line 53 to col. 6 line 32, Figs. 3a-b, col. 5 line 53 to col. 6 line 7, and col. 6 lines 33-47).

Regarding claim 17:

Muller et al. disclose wherein said time-division multiplexed receive control line contains receive control signals further comprising a carrier sense signal (col. 5 lines 25-43).

8. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (6,044,087) in view of Biggs et al. (5,535,398) as applied to claim 1 above, and further in view of Chow et al. (6,169,742).

Regarding claims 13-14:

For claims 13-14 Muller et al. in view of Biggs et al. disclose the method described in paragraph 6 of this office action. Muller et al. in view of Biggs et al. disclose all the subject matter of the claimed invention with the exception of buffering data transmitted from the PHY to the MAC using an elasticity buffer that is at least 27 bits long as in claim 13 and buffering data transmitted from the PHY to the MAC using an elasticity buffer that long enough to buffer an entire frame of data from a data source having a clock with a frequency tolerance of 0.1% as in claim 14.

Chow et al. from the same or similar fields of endeavor teach that it is known to provide the step of buffering data transmitted from the PHY to the MAC using an elasticity buffer that is at least 27 bits long (col. 6 lines 9-27) and that is long enough to buffer an entire frame of data from a data source having a clock with a frequency tolerance of 0.1% (see Fig. 3a and col. 6 lines

9-27). Thus, it would have been obvious to the person having ordinary skill in the art at the time the invention was made to provide the step of buffering data transmitted from the PHY to the MAC using an elasticity buffer that is at least 27 bits long and that is long enough to buffer an entire frame of data from a data source having a clock with a frequency tolerance of 0.1% as taught by Chow et al. in the method of Muller et al. in view of Biggs et al. The motivation for providing the step of buffering data transmitted from the PHY to the MAC using an elasticity buffer that is at least 27 bits long and that is long enough to buffer an entire frame of data from a data source having a clock with a frequency tolerance of 0.1% as taught by Chow et al. in the method of Muller et al. in view of Biggs et al. being that it provides a more robust method of sending and receiving data packets and said more robust packet switching being desirable to achieve more efficient system operation in Muller et al. in view of Biggs et al.

Allowable Subject Matter

9. Claims 2-3, 7-8, 11-12 and 19-20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to

include all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
Crayford et al. disclose optimized MII for 802.3U (100 Base-T) fast Ethernet PHYS.
Bachrach discloses physical layer and data link interface with Ethernet pre-negotiation.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shick C Hom whose telephone number is 571-272-3173. The examiner can normally be reached on Monday to Friday with alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH SH

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